DATA PROCESSING SYSTEM WITH REGISTER STORE/LOAD UTILIZING DATA PACKING/UNPACKING

ABSTRACT OF THE DISCLOSURE

A data processing system (e.g., microprocessor **30**) for packing register data while storing it to memory and unpacking data read from memory while loading it into registers using single processor instructions. The system comprises a memory (**42**) and a central processing unit core (**44**) with at least one register file (**76**). The core is responsive to a load instruction (e.g., LDW_BH[U] instruction **184**) to retrieve at least one data word from memory and parse the data word over selected parts of at least two data registers in the register file. The core is responsive to a store instruction (e.g., STBH_W instruction **198**) to concatenate data from selected parts of at least two data registers into at least one data word and save the data word to memory. The number of data registers is greater than the number of data words parsed into or concatenated from the data registers. Both memory storage space and central processor unit resources are utilized efficiently when working with packed data. A single store or load instruction can perform all of the tasks that used to take several instructions, while at the same time conserving memory space.